Amendments to the Specification

In the Abstract, please amend the following.

~~Test stimulus data is shifted into a first module 3A, and test response data captured in response to a global scan enable signal 27 being activated. Each module comprises a control circuit 59A, 59B, for example an OR gate, for controlling whether or not the global scan enable signal 27 is passed to its respective module. The control circuits 59A, 59B are controlled by a dedicated bypass signal 61 A, 61 B, respectively. The dedicated bypass signals 61 A, 61 B act as control signals for controlling whether or not the local scan enable signals 60A and 60B mirror the global scan enable signal 27. This enables the global scan enable signal 27 to be kept high for one or more particular modules that are not being tested, by maintaining the dedicated bypass signal 61A or 61B high for those particular modules, such that they are placed in a transport mode of operation. The invention allows test pattern data to be processed in a pipelined manner, such that modules located prior to the module being tested contain the next set of test stimulus data from a series of test stimulus data, and modules located after the module to be tested contain test response data from previous tests.~~

According to an example embodiment of the present invention, there is a test access architecture for testing modules in an electronic circuit. The test access architecture includes a test access mechanism (TAM) having a plurality of modules connected in series thereto; the test access mechanism is arranged to transport test stimulus data to, and test response data from a module being tested. A global enable signal is provided for placing the modules in a test mode. A control circuit is provided between the global enable signal and an associated module; wherein the control circuit is arranged to control whether or not the global enable signal is passed to its associated module.

In the Specification, page 6, lines 1-14, please amend the following.

~~According to the present invention, there is provided a test access architecture for testing modules in an electronic circuit, the test access architecture comprising:~~

~~a test access mechanism (TAM) having a plurality of modules connected in series thereto, the test access mechanism arranged to transport test stimulus data to, and test response data from a module being tested;~~

~~a global enable signal, the global enable signal provided for placing the modules in a test mode; and~~

~~a control circuit provided between the global enable signal and an associated module, wherein the control circuit is arranged to control whether or not the global enable signal is passed to its associated module.~~

According to an example embodiment of the present invention, there is a test access architecture for testing modules in an electronic circuit. The test access architecture comprises a test access mechanism (TAM) having a plurality of modules connected in series thereto; the test access mechanism is arranged to transport test stimulus data to, and test response data from a module being tested. A global enable signal is provided for placing the modules in a test mode. A control circuit is provided between the global enable signal and an associated module; wherein the control circuit is arranged to control whether or not the global enable signal is passed to its associated module.

In the Specification, page 6, lines 30-35 through page 7, lines 1-9, please amend the following.

~~According to another aspect of the invention, there is provided a method of testing a module in an electronic circuit, the module being one of a plurality of modules connected in series to a test access mechanism (TAM), the test access mechanism arranged to transport test stimulus data to a module being tested, and to transport test response data from the module being tested, the method comprising the steps of:~~

~~unloading a first set of test stimulus data into the module being tested;~~

~~testing the module in response to a global enable signal being activated;~~

~~unloading test response data captured from the module being tested; wherein, during the testing step, other modules connected to the test access mechanism (TAM) are placed in a transport mode of operation, such that the other modules do not corrupt a second set of test stimulus data being loaded into, or previous test response data being unloaded from, the module under test.~~

According an another example embodiment of the present invention, there is a method of testing a module in an electronic circuit. The module is one of a plurality of modules connected in series to a test access mechanism (TAM); the test access mechanism is arranged to transport test stimulus data to a module being tested, and to transport test response data from the module being tested. The method comprises loading a first set of test stimulus data into the module being tested. In response to a global signal being activated, the module is tested. From the module being tested, captured test response data are unloaded. Wherein, during the testing step, other modules connected to the test access mechanism (TAM) are placed in a transport mode of operation, such that the other modules do not corrupt a second set of test stimulus data being loaded into, or previous test response data being unloaded from, the module under test.